ABSTRACT OF THE DISCLOSURE

[0093] Apparatus for generating an additional voltage drop to reduce the dangerously high voltage drop across an ESD-sensitive ultra-thin gate oxide of a MOS input device. The apparatus are designed to minimally interfere with the circuit requirements for normal operation. Specifically, The MOS input device is coupled between a pad and the logic core circuitry of the IC. In one embodiment, a voltage-drop element, such as a resistive element, inductor, or pass-gate MOS device, is coupled between the source of the MOS input device and a voltage line. Alternatively, the voltage-drop element may be coupled to the bulk, gate, and/or drain of the MOS input device. In another embodiment, the voltage-drop device may be an active device, which pumps up the potential at least one of the source, bulk, or drain regions of the input device from the ESD clamp.